In the Claims:

1. – 20. Canceled.

21. (Previously Presented) A method of producing a memory cell, comprising:

providing a trench capacitor in a substrate;

providing a dielectric layer on an upper portion of the trench capacitor;

providing a transistor coupled to said trench capacitor, including etching the substrate to produce a transistor trench adjacent the trench capacitor, and providing in the transistor trench a portion of a gate of the transistor; and

said etching step including using the dielectric layer as an etch mask.

22. (Previously Presented) The method of Claim 21, wherein a width of the transistor trench is less than a lithographic groundrule.

23. (Previously Presented) The method of Claim 22, including providing a portion of the gate of the transistor outside of the transistor trench, said portion having a width greater than the width of the transistor trench.

24. (Previously Presented) The method of Claim 22, including providing a portion of the gate of the transistor outside of the transistor trench, said portion having a width equal to the lithographic groundrule.

25. (Previously Presented) The method of Claim 21, wherein the gate is doped polysilicon.

26. (Previously Presented) The method of Claim 21, including providing a cap layer over a further portion of the gate that is outside of the transistor trench.

27. (Previously Presented) The method of Claim 21, including providing a salicide layer over a further portion of the gate that is outside of the transistor trench.

28. (Previously Presented) The method of Claim 27, including providing a cap layer over the further portion of the gate.

29. (Previously Presented) The method of Claim 21, wherein the dielectric layer is silicon oxide.

30. (Previously Presented) The method of Claim 29, wherein the gate is doped polysilicon.

31. (Previously Presented) The method of Claim 21, including providing a portion of the gate of the transistor outside of the transistor trench, said portion having a width greater than the width of the transistor trench.

32. (Previously Presented) The method of Claim 21, including providing a portion of the gate of the transistor outside of the transistor trench, said portion having a width equal to a lithographic groundrule.

33. (Previously Presented) An article of manufacture including an integrated circuit having a memory cell produced according to the method of Claim 21.